III. REMARKS

The Examiner has refused to consider document JP 2002-171303, filed with Applicants' Information Disclosure Statement (IDS) on March 16, 2004, on the grounds that the IDS did not include a concise explanation of its relevance (Office Action, dated January 30, 2006, at 2, lines 3-7). The Examiner's attention is directed to page 1, lines 24-26, of Applicant's March 16th, 2004 IDS, which explains that document JP 2002-171303 is discussed in Applicants' specification. The Examiner's attention is drawn to paragraph [0005] of Applicants' specification, which provides a concise explanation of the relevance of document JP 2002-171303. Therefore, Applicants respectfully request that the document JP 2002-171303 be properly considered by the Examiner.

Applicants respectfully traverse the Examiner's objection to the use of abbreviations in the claims (Office Action, dated January 30, 3006, at 2, lines 9-11) because it is a well-established proposition that an applicant may be his own lexicographer and that the written description of the invention should be considered to determine whether the applicant has ascribed a certain meaning to the claim terms. Digital Biometrics Inc. v. Identix Inc., 47 U.S.P.Q.2d 1418, 1424 (Fed. Cir. 1998).

In this case, Applicants have ascribed certain meaning to the abbreviations used in the claims (i.e., SDIO, SD, R/W FIFO, RFIFO, WFIFO, I/O) as described in the written description, and as is in accordance with the custom of the particular art of the invention. Applicants assert that if all abbreviations are replaced with their corresponding longhand equivalents that the language of the claims will become unwieldy, which will detract from the clarity of the claims. To the degree that Applicants believe the abbreviations may be replaced without compromising clarity, Applicants have done so. Furthermore, the replacement of any abbreviation with its equivalent unabbreviated form has no limiting effect whatsoever on the scope of the present claims.

Claims 3 and 7 have been canceled without prejudice. Claims 1, 2, 4-6 and 8-20 have been amended, and new claim 21 has been added. In particular, the following abbreviations "SD," "SDIO," and "R/W FIFO," respectively, have been replaced by their equivalent unabbreviated form --Secure Digital--, --Secure Digital Input Output--, and --First-in, First-out-- as supported by paragraphs [0003], [0002] and [0008] of the specification as originally filed. Claim 5 has been amended to replace "RFIFO" and "WFIFO" with --First-In, First-out device-- and --First-in, First-out device--, respectively, as supported by paragraphs [0008], [0010], [0048] of the specification as originally filed.

Independent claims 1, 12 and 17 have been amended to additionally recite "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as supported by Figure 1, paragraphs [0029], [0031] and claim 3 of the application as originally filed. Independent claims 1, 12 and 17 have also been amended to additionally recite that the SDIO controller includes "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces" as supported by paragraph [0031] and [0052] of the specification as originally filed.

Claim 6 has been amended to replace "read memory" with --read First-in, First-out device-- and to replace "write memory" with --write First-in, First-out device-- as supported by paragraph [0048] of the specification as originally filed. Claim 6, and claim 4, have also been amended to recite that the data is to be "sent out from the Secure Digital Input Output host" as supported by paragraph [0058] of the originally filed specification.

Claims 8 and 16 have been amended to depend upon claims 1 and 14, respectively. Claims 11 and 20 have been amended to recite "arbitrary write data in a digital system" as supported by paragraph [0003] of the application as originally filed. Claim 19, which

depends upon claim 18, has been amended to recite a "wireless communications module" in accordance with the preamble of claim 18.

Claim 20 has been additionally amended to replace, in step (f), "SD memory" with -- registers-- as supported by paragraph [0055] of the specification as originally filed.

New claim 21, which depends upon claim 1, further recites "wherein the temporary memory comprises one First-in, First-out device for writing data and three First-in, First-out devices for reading data" as supported on page 16, lines 9-12, of the specification as originally filed.

A. The Invention

The present invention pertains broadly to SDIO technology such as is used to construct and operate various electronic devices. In particular, in accordance with an apparatus embodiment of the present invention, a Secure Digital Input Output controller having a single-chip semiconductor device connecting a Secure Digital Input Output-compliant Secure Digital Input Output host device with a plurality of applications via a secure digital bus is provided wherein the Secure Digital Input Output controller includes the features recited in independent claim 1. In accordance with another apparatus embodiment of the present invention, a Secure Digital Input Output wireless communications card is provided that includes the features recited in independent claim 12. In accordance with yet another apparatus embodiment of the present invention, a Secure Digital Input Output wireless communications module is provided that includes the features recited by independent claim 17.

In accordance with a method embodiment of the present invention, a method of transmitting write data from a Secure Digital Input Output host device to a Secure Digital Input Output application is provided that includes the steps recited by independent claim 20.

Various other embodiments, in accordance with the present invention, are recited by the dependent claims. An advantage of the method and apparatus embodiments of the present invention is that a highly versatile SDIO controller, or method of SDIO control, is provided that enables interface of an SDIO host with a plurality of applications and that provides other devices benefit from application of the versatile SDIO controller or method of SDIO control.

B. The Rejections

Claims 11, 16 and 20 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

Claims 1-10, 12-15 and 17-19 stand rejected under 35 U.S.C. § 102(b) as anticipated by Ito (U.S. Patent Application Publication No. US 2001/0006902 A1, hereafter the "Ito Publication").

Claims 11 and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the Ito Publication in view of Fackenthal (U.S. Patent 6,748,482 B1, hereafter the "Fackenthal Patent"). Claim 16 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the Ito Publication in view of Hanson et al. (U.S. Patent Application Publication No. US 2004/0225796 A1, hereafter the "Hanson Publication").

Applicants respectfully traverse the rejections and respectfully request reconsideration of the above-captioned application for the following reasons.

C. Applicants' Arguments

In view of the present amendment, claims 1, 2, 4-6 and 8-20 are now in compliance with 35 U.S.C. § 112.

D. The Section 102 Rejection

Anticipation under 35 U.S.C. § 102 requires showing the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). In this case, the Examiner has failed to establish a prima facie case of anticipation because the Ito Publication does not teach each and every limitation of the claimed invention, arranged as in the claims.

i. The Ito Publication

The Ito Publication teaches an "IC card with radio interface function, antenna module and data processing apparatus using the IC card," which as shown in Figure 2 is an SD memory card (10) that contains an RF circuit (20), a controller LSI (21) and a flash memory (22), (See Abstract). The Ito Publication teaches that the RF circuit is connected to an antenna module (21) attached to the SD memory card (10), the controller LSI (21) executes radio interface control and interface control for the SD memory card, and that by running a protocol control program and an SD memory card interface control program stored in ROM (21b) using an MPU (21a), the controller LSI (21) executes upper-protocol control and SD memory interface control (See Abstract). The SD memory card (10) taught by the Ito Publication has a memory interface (21e) and an SD card interface (21f) as shown in Figure 2.

However, the Ito Publication does not teach, or suggest, that its SD memory card includes (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces" as recited by independent claims 1, 12 and 17 of the present application.

While the Ito Publication teaches an SD memory card embodiment in Figure 2 having a memory interface (21e) and an SD card interface (21f) for a plurality of pins (col. 2, lines 34-40), it does not teach, or suggest, an SDIO controller comprising (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17 of the present application. Likewise, while another SD memory card embodiment is shown in Figure 8 of the Ito Publication, this embodiment includes a memory interface (51e), an SD card interface (51f), and an SD-BT interface (56f) for connecting the Bluetooth function expansion module (50) to the SD memory card (10e). However, the embodiment shown in Figure 8 of the Ito Publication also does not teach, or suggest, "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited by independent claims 1, 12 and 17.

In other words, the Ito publication does not teach, or suggest, an SDIO controller that includes "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface," which requires more than one such interface. The "other devices" (21g) of Figure 2 are not defined by the Ito Publication and are not shown to connect to an external circuit (col. 2, lines 34-40), therefore the other devices (21f) cannot be reasonably interpreted to be a PCMCIA interface, a PC card bus interface, or a UART interface. Furthermore, the "application interfaces" as recited in the present claims 1, 12 and 17, do not include a "memory interface." The "application interfaces" recited in claims 1, 12 and 17 are selected from the group of a PCMCIA interface, a PC card bus interface, and a UART interface, which are common and general interfaces that make it possible for the apparatus embodiments of the present invention to not only select applications for use, but also minimizes development costs and labor efforts related to

engineering a card system fully compatible with the complicated SDIO standard (See original specification, page 3, paragraph [0009]).

As admitted by the Examiner (Office Action, dated January 30, 2006, at 6, lines 14-15, and at 7, lines 1-5), the Ito Publication does not teach, or suggest, (c) that the "microcontroller unit operates to access non-contiguous registers via an application interface" as recited by claim 11; (d) "one or more additional applications selected from the group consisting of a global positioning system and a personal handyphone system" as recited by claim 16; and (e) the step of "accessing non-contiguous register addresses of registers in the Secure Digital Input Output application via the application interface by using the microcontroller unit..." as recited by independent claim 20.

The Ito Publication also does not teach, or suggest, "the temporary memory comprises one First-in, First-out device for writing data and three First-in, First-out devices for reading data" as recited by new claim 21.

For all of the above reasons, the Examiner has failed to establish a prima facie case of anticipation against the claims of the above-captioned application.

E. The Section 103 Rejection

A prima facie case of obviousness requires a showing that the scope and content of the prior art teaches each and every element of the claimed invention, and that the prior art provides some teaching, suggestion or motivation to combine the references to produce the claimed invention. In re Oetiker, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992); In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). In this case, the Examiner has failed to establish a prima facie case of obviousness against the instant claims because neither the Ito Publication, the Fackenthal Patent, nor the Hanson Publication teach, or suggest, (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data

between the temporary memory and the application interfaces" and (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17 of the present application.

i. The Ito Publication

The Ito Publication has been discussed above.

ii. The Fackenthal Patent

The Fackenthal Patent teaches "multiple non-contiguous block erase in flash memory," wherein a flash memory block erase operation permits multiple blocks to be erased simultaneously, even if the blocks are non-contiguous (See Abstract). However, the Fackenthal Patent does not teach, or suggest, (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces" and (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17 of the present application.

iii. The Hanson Publication

The Hanson Publication teaches "expandable miniature accessory card for handheld computer" wherein an SDIO module (130) is coupled to an expansion slot (140) in the housing (120) of a handheld computer (100), (page 2, first col., lines 21-25). The Hanson Publication further teaches that the SDIO module (130) is an SDIO card having an accessory device coupled therewith, such as a Bluetooth receiver, a digital camera, an audio player, and FM or television tuner, a local area network card, a global positioning system receiver, a

voice recorder, and a pedometer (page 2, first col., lines 36-42). However, the Hanson Patent does not teach, or suggest, (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces" and (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17 of the present application.

iv. Combinations of Ito, Fackenthal and Hanson

Because neither the Ito Publication, the Fackenthal Patent, nor the Hanson Publication teach, or even suggest, (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces" and (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17 of the present application, each combination of these documents will fail to teach these features of the claimed invention. Therefore, the Examiner has failed to establish a prima facie case of obviousness against independent claims 1, 12 and 17.

v. Claim 20

The Examiner admits that the Ito Publication fails to teach, or suggest, all of the subject matter of claim 20 (Office Action, dated January 30, 2006, at 6, lines 6-24). However, the Examiner has not demonstrated that the Ito Publication teaches any of the subject matter of claim 20. Instead, the Examiner makes the flawed conclusion that "[w]ith respect to claim 20, it is of the same scope as the combination of claims 1, 11 and 12, and thus is rejected under the same rationale" (Office Action, dated January 30, 2006, at 6, lines 23-24). The Examiner's conclusion that claim 20 is of the "same scope" as the combination

of claims 1, 11 and 12 is facially incorrect. Consequently, the Examiner's inference that a rejection of claims 1, 11 and 12 would necessarily establish a prima facie case of obviousness against claim 20 is also facially incorrect.

Claims 1 and 11 recite a "Secure Digital Input Output controller." Claim 12 recites a "Secure Digital Input Output wireless communications card." Claims 1 and 11 and 12 relate to various apparatus embodiments in accordance with the present invention. On the other hand, claim 20 recites a "method of transmitting write data from a Secure Digital Input Output host device to a Secure Digital Input Output application," which pertains to a method embodiment in accordance with the present invention. The scope of subject matter covered by claim 20, a method embodiment, is not equivalent to a combination of the subject matter of claims 1, 11 and 12, which relate to apparatus embodiments. On its face, the Examiner's conclusory analysis of the subject matter of claim 20 is flawed as well as the erroneously inferred Section 103 rejection. The Examiner's Section 103 rejection of claim 20 is untenable and must be withdrawn for the following reasons.

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness, and only if that burden is met, does the burden of coming forth with evidence or argument shift to the applicant. In re Rijckaert, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). Furthermore, where the PTO asserts that there is an explicit or implicit teaching or suggestion in prior art, the PTO must indicate where in the reference the teaching or suggestion appears. In re Rijckaert, 28 U.S.P.Q.2d at 1957.

In this case, the Examiner has made no attempt whatsoever to show that any of the subject matter of claim 20 is taught by any reference. The Examiner has simply not met the initial burden of establishing a prima facie case of obviousness against claim 20.

Applicants assert that neither the Ito Publication, the Fackenthal Patent nor the Hanson Publication teach, or suggest, either alone or in combination, the following

combination of steps recited by claim 20: (a) connecting a Secure Digital Input Output application with a Secure Digital Input Output host device, wherein the Secure Digital Input Output application comprises a Secure Digital Input Output controller having a Secure Digital interface and an application interface; (b) receiving a write command from the Secure Digital Input Output host device via the Secure Digital interface and interpreting the command; (c) generating a command response signal using the Secure Digital interface and sending the command response signal to the Secure Digital Input Output host device; (d) after the Secure Digital Input Output host device receives the command response signal, transmitting data from the host device to the Secure Digital Input Output controller via the Secure Digital interface, wherein the transmitted data includes at least a register read/write address, a selected type of operation, a quantity of data, and arbitrary write data in a digital system; (e) decoding the transmitted data using a microcontroller unit of the Secure Digital Input Output controller; and (f) accessing non-contiguous register addresses of registers in the Secure Digital Input Output application via the application interface by using the microcontroller unit so data sent from the Secure Digital Input Output host device is written into the registers of the Secure Digital Input Output application.

For all of the above reasons, the Examiner has not establishes a prima facie case of obviousness against any of the claims of the above-captioned application.

IV. CONCLUSION

Claims 1, 2, 4-6 and 8-20 are now in compliance with 35 U.S.C. § 112. The rejection of independent claims 1, 12 and 17, either under Section 102(b) or Section 103(a), is untenable and must be withdrawn because neither the Ito Publication, the Fackenthal Patent, nor the Hanson Publication, teach, or suggest, (a) "a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary

memory and the application interfaces" and (b) "application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface" as recited in independent claims 1, 12 and 17. With respect to independent claim 20, the Examiner's contention that claim 20 has the "same scope" as the combination of claims 1, 11 and 12 is erroneous because claim 20 pertains to a method embodiment and has a very different scope than that of claims 1, 11 and 12, which pertain to various apparatus embodiments of the invention. Consequently, the Examiner's inference that a rejection of claim 11 should pertain to claim 20 is untenable and must be withdrawn because the Examiner has not demonstrated that any reference or combination of references teach, or suggest, the subject matter of claim 20.

For all of the above reasons, claims 1, 2, 4-6 and 8-21 are in condition for allowance, and a prompt notice of allowance is earnestly solicited.

The below-signed attorney for Applicants welcomes any questions.

Respectfully submitted,

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